Patent claims

1. A circuit arrangement for electrically generating a ringing impedance in telephone terminals by means of at least one transistor (T1; T2, T3) and a capacitor (C; C1, C2), the ringing impedance being adaptable by controlling the resistance of the transistor, having a ringing alternating voltage (V~) which can be tapped between a first input terminal (a) and a second input terminal (b), characterized in that a digital controller (2, 4, 8; 2', 2'', 4, 8', 8'') is provided for setting the ringing impedance, said controller adapting the ringing impedance to the given conditions by generating from the ringing alternating voltage (V~) a control voltage (VSt) for controlling the transistor (T1),
the digital controller (2, 4, 8, 2', 2'', 4, 8', 8'') has a programmable digital filter (4), and
the transmission function of the digital filter (4) can be set by programming the associated filter coefficients.

2. The circuit arrangement as claimed in claim 1, characterized in that the digital filter (4) is a component of a programmable digital signal processor (4) or microprocessor.

3. The circuit arrangement as claimed in one of claims 1 or 2, characterized in that a digital power inverter circuit (3) is connected upstream of the digital filter (4) and a digital rectifier circuit (5) is connected downstream of the digital filter.

4. The circuit arrangement as claimed in one of the preceding claims, characterized by

- a rectifier circuit (1) for rectifying the ringing alternating voltage (V~),
- a capacitor (C) which is connected between an input terminal (a) and rectifier circuit (1),

- a transistor (T1) which is arranged by means of its load path between the outputs (12, 13) of the rectifier circuit (1),
- a first and second voltage (Va, Vb), which are rectified from the ringing alternating voltage (V~) by means of the rectifier circuit (12), being fed to the controller (2, 4, 8), and
- the controller (2, 4, 8) making available a control voltage (VSt) for driving the transistor (T1).

5. The circuit arrangement as claimed in one of the preceding claims, characterized in that the controller (2, 4, 8) has an analog integrator circuit (8) which is connected upstream of the transistor (T1) and which makes available an output signal (VSt) which is integrated from the difference between a first input voltage (VI) and a second input voltage (Vb) and which drives the transistor (T1).

6. The circuit arrangement as claimed in one of the preceding claims, characterized in that a voltage divider (R2, R3) is provided which makes available a component voltage from the voltage (Va) which is present at the one output (12) of the rectifier circuit (1).

7. The circuit arrangement as claimed in claim 3, characterized in that the digital power inverter circuit (3), the digital filter (4) and the digital rectifier circuit (5) are together integrated on a semiconductor chip of digital design.

8. The circuit arrangement as claimed in one of claims 3 to 7, characterized in that an analog/digital converter (2) is provided which is connected upstream of the digital power inverter circuit (3), and a digital/analog converter (6) is provided which is connected downstream of the digital rectifier circuit (5), the analog/digital converter (2), the digital/analog converter (6) and the analog integrator

circuit (8) being together integrated on a semiconductor chip of analog design.

9. The circuit arrangement as claimed in claim 1 or 2, characterized in that

- a first capacitor (C1), the load path of a first transistor (T2) and a first resistor (R10) are arranged in series between the first terminal (a) and a reference potential (VSS),
- a second capacitor (C2), the load path of a second transistor (T3) and a second resistor (R20) are arranged in series between the second terminal (b) and the reference potential (VSS),
- a first and a second input potential (Va~) of the ringing alternating voltage (V~) being fed to the controller (2', 2'', 4, 8', 8''), and
- the controller (2', 2'', 4, 8', 8'') making available a first control voltage (VSt1) for driving the first transistor (T2) and a second control voltage (VSt2) for driving the second transistor (T3).

10. The circuit arrangement as claimed in claim 9, characterized in that the controller (2', 2'', 4, 8', 8'')

- has a first analog integrator circuit (8') which is connected upstream of the first transistor (T2) and which makes available an output signal (VSt1) which is integrated from the difference between a first input voltage (VI1) and a second input voltage (Vam) and which drives the first transistor (T2), and
- has a second analog integrator circuit (8'') which is connected upstream of the second transistor (T3) and which makes available an output signal (VSt2) which is integrated from the difference between a third input voltage (VI2) and a fourth input voltage (Vbm) and which drives the second transistor (T3).

11. The circuit arrangement as claimed in claim 9 or 10, characterized in that a first voltage divider (R30, R50) is provided which makes available a first component voltage from the first potential (Va~) of the ringing alternating voltage (V~), and
a second voltage divider (R40, R60) is provided which makes available a second component voltage from the second potential (Vb~) of the ringing alternating voltage (V~).

12. The circuit arrangement as claimed in claim 10 or 11, characterized in that at least one analog/digital converter (2', 2''), which is connected upstream of the digital filter (4), is provided, and at least one digital/analog converter (6', 6''), which is connected downstream of the digital rectifier circuit (5), is provided, the analog/digital converters (2', 2''), the digital/analog converters (6', 6'') and the analog integrator circuits (8', 8'') being together integrated on a semiconductor chip of analog design.

13. The circuit arrangement as claimed in one of claims 4 to 12, characterized in that at least one of the transistors (T1; T2, T3) is embodied as an n-channel-MOSFET.